REMARKS

Claims 1-11 and 14-17 are pending in the present application. In the Office Action mailed June 25, 2007, Claims 1-10 and 14-17 are rejected under 35 U.S.C. § 102(b) as being anticipated by Johnson, U.S. Patent No. 5,898,701. Claim 11 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Johnson in view of Lindholm, U.S. Patent No. 6,553,523.

In response to the rejection of the claims, Applicant has amended each of the independent claims to overcome the rejection. In particular, Applicant has amended each of the independent claims to more clearly indicate that configuration data is coupled to a boundary scan register by way of an input/output port, and that a connection to the input/output pin of the programmable logic device is verified. Applicant has amended independent Claim 1 to include a step of "coupling configuration process signals to an input/output pin of the programmable logic device," and indicate that the boundary scan registers are used "to capture the configuration process signals received at the input/output pin of the programmable logic device during the configuration process." Finally, Applicant has further added a step of "verifying a connection to the input/output pin of the programmable logic device coupled to receive the configuration process signals."

Applicant has similarly amended Claim 9 to indicate that the programmable logic device has boundary scan registers which are "coupled to receive a configuration bitstream by way of an input/output pin." Applicant has also amended Claim 9 to indicate that the configuration device provides the configuration bitstream to the programmable logic device "by way of the I/O pin." Applicant has corrected a minor inadvertent clerical error related to the I/O pins controlled by the configuration analyzer. Finally, Applicant has amended Claim 9 to indicate that the JTAG chain enables "verifying a connection to the input/output pin of the programmable logic device coupled to receive the configuration bitstream."

Applicant has also amended Claim 16 to include a step of "coupling configuration process signals to an input/output pin of the programmable logic device." Applicant has further amended the step of using the boundary scan registers to indicate that they are used to "capture the configuration process signals received at

the input/output pin of the programmable logic device." Applicant has also added a step of "verifying a connection to the input pin of the programmable logic device coupled to receive the configuration process signals."

Finally, Applicant has amended Claim 17 to include "means for receiving configuration process signals by way of an input/output pin of the programmable logic device," and "means for verifying a connection to the input/output pin of the programmable logic device coupled to receive the configuration process signals." Applicant has also amended Claim 17 to indicate that the means for capturing configuration process signals captures configuration process signals "received at the input/output pin in boundary scan registers."

Support for the above described amendments to each of the claims may be found at least in Fig. 3, and paragraphs [0028]-[0031] and [0035]-[0036].

Applicant respectfully submits that the claims as amended clearly distinguish over Johnson. According to Applicant's claims, the use of a boundary scan register enables verifying a connection to an input/output pin of the programmable logic device coupled to receive configuration process signals at the input/output pin. There is no teaching or suggestion in Johnson that a boundary scan register of Johnson is coupled to an input/output pin receiving configuration process signals. In contrast, Johnson merely teaches that a boundary scan register is coupled to either a test data input (TDI) signal, a test clock (TCK) or decoded test mode select (TMS) signal. There is also no teaching or suggestion that the circuit of Johnson enables verifying a connection to an input/output pin of the programmable logic device coupled to receive the configuration process signals. Applicant respectfully submit that each of the independent Claims 1, 9, 16 and 17 as amended clearly distinguish over Johnson, and respectfully request reconsideration of the rejection. Applicant also submits that dependent Claims 2-8, 10-11, and 14-15 are allowable for the same reasons that the independent claims are believed allowable.

In response to the rejection of Claim 11, Applicant respectfully submits that Claim 11 is allowable over the combination of references for the same reasons that Claim 9 is believed allowable over Johnson alone. That is, Lindholm is cited for disclosing that a field programmable gate array is a programmable logic device.

However, Lindholm also fails to disclose or suggest a configuration analyzer analyzing configuration process signals stored in boundary scan registers of the programmable logic device during the configuration process, as claimed in independent Claim 9. Applicant respectfully requests reconsideration of Claim 11.

Conclusion

Applicant believes that Claims 1-11 and 14-17 are in condition for allowance, and allowance of the application is therefore requested. If action other than allowance is contemplated by the Examiner, the Examiner is respectfully requested to telephone Applicant's attorney, Justin Liu, at 408-879-4641.

Respectfully submitted,

Justin Liu
Attorney for Applicant
Reg. No. 51,959

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on August 20, 2007.

Katherine Stofer
Name

Signature